# DUAL OUTPUT BOOST WLED DRIVER USING SINGLE INDUCTOR

## FEATURES

- 2.5-V to 6-V Input Voltage Range
- Two Outputs Each up to 27 V
- 0.7-A Integrated Switch
- Built-In Power Diode
- 1.2-MHz Fixed PWM Frequency
- Individually Programmable Output Current
- Input-to-Output Isolation
- Built-In Soft Start
- Overvoltage Protection
- Up to 83% Efficiency
- Up to 30-kHz PWM Dimming Frequency
- Available in a 10-Pin, 3- × 3-mm QFN Package

## APPLICATIONS

- Sub and Main Display Backlight in Clam Shell Phones
- Display and Keypad Backlight
- Up to 14 WLED Driver

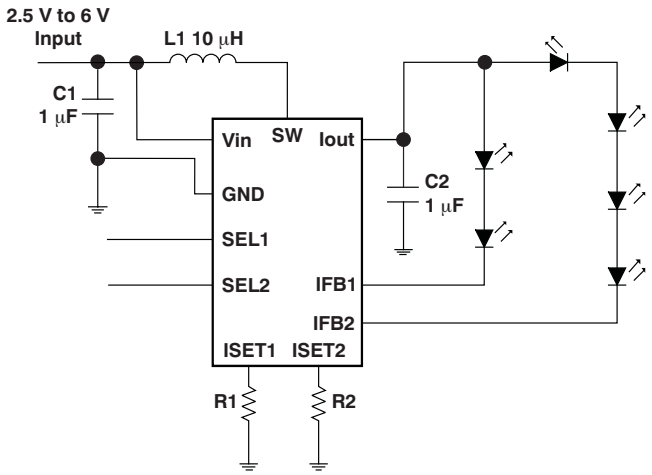
## DESCRIPTION

The TPS61150/1 is a high-frequency boost converter with two regulated current outputs for driving WLEDs. Each current output can be individually programmed through external resistors. There is a dedicated selection pin for each output, so the two outputs can be turned on separately or simultaneously. The output current can be reduced by a pulse width modulation (PWM) signal on the select pins or an analog voltage on the ISET pins, resulting in PWM dimming of the WLEDs. The boost regulator runs at a 1.2-MHz fixed switching frequency to reduce output ripple and avoid audible noises associated with PFM control.

The two current outputs are ideal for driving WLED backlights for the sub- and main displays in clamshell phones. The two outputs can also be used for driving display and keypad backlights. When used together, the two outputs can drive up to 14 WLEDs for one large display.

In addition to the small inductor, small capacitor and 3-mm x 3-mm QFN package, the built-in MOSFET and diode eliminate the need for any external power devices. Overall, the IC provides an extremely compact solution with high efficiency and plenty of flexibility.

## TYPICAL APPLICATION

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION

| $T_A$ | PACKAGE(1) | OVP (Typ.) | PACKAGE MARKING |
|---|---|---|---|
| –40 to 85°C | TPS61150DRCR | 28 V | BCQ |
| –40 to 85°C | TPS61151DRCR | 22 V | BRH |
| –40 to 85°C | TPS61150DRCT | 28 V | BCQ |
| –40 to 85°C | TPS61151DRCT | 22 V | BRH |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

| | VALUE | UNIT |
|---|---|---|
| Supply voltages on pin VIN(2) | –0.3 to 7 | V |
| Voltages on pins SEL1/2, ISET1/2(2) | –0.3 to 7 | V |
| Voltage on pin IOUT, SW, IFB1 and IFB2(2) | 30 | V |
| Continuous power dissipation | See Dissipation Rating Table | |
| Operating junction temperature range | –40 to 150 | °C |
| Storage temperature range | –65 to 150 | °C |
| Lead temperature (soldering, 10 sec) | 260 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

## DISSIPATION RATINGS

| PACKAGE | $R_{\theta JA}$ | $T_A \le 25°C$ POWER RATING | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING |
|---|---|---|---|---|
| QFN (1) | 270°C/W | 370 mW | 204 mW | 148 mW |
| QFN(2)(2 | 48.7°C/W | 2.05 W | 1.13 W | 821 mW |

(1) Soldered PowerPAD on a standard 2-layer PCB without vias for thermal pad.
(2) Soldered PowerPAD on a standard 4-layer PCB with vias for thermal pad .

## RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted).

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_I$ | Input voltage range | 2.5 | | 6 | V |
| $V_O$ | Output voltage range | Vin | | 27 | V |
| L | Inductor(1) | | 10 | | µH |
| $C_{IN}$ | Input capacitor(1) | 1 | | | µF |
| $C_O$ | Output capacitor(1) | 1 | | | µF |
| $T_A$ | Operating ambient temperature | –40 | | 85 | °C |
| $T_J$ | Operating junction temperature | –40 | | 125 | °C |

(1) See the *Application Information* section for further information.


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## ELECTRICAL CHARACTERISTICS

At $V_I$ = 3.6 V, SELx = $V_{IN}$, Rset = 80 kΩ, $V_{IO}$ = 15 V, and $T_A$ = –40°C to 85°C. Typical values are at $T_A$ = 25°C (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | |
| $V_I$ | Input voltage range | | 2.5 | | 6 | V |
| $I_Q$ | Operating quiescent current into Vin | Device PWM switching no load | | | 2 | mA |
| $I_{SD}$ | Shutdown current | SELx = GND | | | 1.5 | µA |
| $V_{UVLO}$ | Undervoltage lockout threshold | Vin falling | | 1.65 | 1.8 | V |
| $V_{hys}$ | Undervoltage lockout hysterisis | | | 70 | | mV |
| **ENABLE AND SOFT START** | | | | | | |
| $V_{(selh)}$ | SEL logic high voltage | $V_{IN}$ = 2.7 V to 6 V | 1.2 | | | V |
| $V_{(sell)}$ | SEL logic low voltage | $V_{IN}$ = 2.7 V to 6 V | | | 0.4 | V |
| $R_{(en)}$ | SEL pull down resistor | | 300 | 700 | | kΩ |
| $T_{off}$ | SEL pulse width to disable | SELx high to low | 40 | | | ms |
| $K_{ss}$ | IFB soft start current steps | | | 16 | | |
| $T_{ss}$ | Soft start time step | Measured as clock divider | | 64 | | |
| $T_{ss_en}$ | Soft start enable time | Time between falling and rising of two adjacent SELx pulses | 40 | | | ms |
| **CURRENT FEEDBACK** | | | | | | |
| $V_{(ISET)}$ | ISET pin voltage | | 1.204 | 1.229 | 1.254 | V |
| $K_{(ISET)}$ | Current multiplier | $I_{OUT}/I_{SET}$ | 820 | 900 | 990 | |
| $K_M$ | Current matching | In reference to the average of two output current | -6 | | 6 | % |
| $V_{(IFB)}$ | IFB Regulation voltage | | 300 | 330 | 360 | mV |
| $V_{(IFB_L)}$ | IFB low threshold hysteresis | | | 60 | | mV |
| $Ti_{sink}$ | Current sink settle time measured from SELx rising edge(1) | | | | 6 | µs |
| $I_{lkg}$ | IFB pin leakage current | IFB voltage = 25 V | | | 1 | µA |
| **POWER SWITCH AND DIODE** | | | | | | |
| $r_{DS(on)}$ | N-channel MOSFET on-resistance | $V_{IN}$ = $V_{GS}$ = 3.6 V | | 0.6 | 0.9 | Ω |
| $I_{(LN_NFET)}$ | N-channel leakage current | $V_{DS}$ = 25 V | | | 1 | µA |
| $V_F$ | Power diode forward voltage | $I_D$ = 0.7 A | | 0.83 | 1.0 | V |
| **OC AND OVP** | | | | | | |
| $I_{LIM}$ | N-Channel MOSFET current limit | Dual output, $I_{OUT}$ = 15 V, D=76% | 0.75 | 1.0 | 1.25 | A |
| | | Single output , $I_{OUT}$ = 15 V, D = 76% | 0.40 | 0.55 | 0.7 | |
| $I_{(IFB_MAX)}$ | Current sink max output current | IFB = 330 mV | 35 | | | mA |
| $V_{OVP}$ | Overvoltage threshold | TPS61150 | 27 | 28 | 29 | V |
| | | TPS61151 | 21 | 22 | 23 | |
| $V_{OVP(hys)}$ | Overvoltage hysteresis | TPS61150 | | 550 | | mV |
| | | TPS61151 | | 440 | | |
| **PWM AND PFM CONTROL** | | | | | | |
| $f_S$ | Oscillator frequency | | 1.0 | 1.2 | 1.5 | MHz |
| $D_{max}$ | Maximum duty cycle | $V_{FB}$ = 1 V | 90 | 93 | | % |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{shutdown}$ | Thermal shutdown threshold | | | 160 | | °C |
| $T_{hys}$ | Thermal shutdown threshold hysteresis | | | 15 | | °C |

(1) This specification determines the minimum on time required for PWM dimming for desirable linearity. The maximum PWM dimming frequency can be calculated from the minimum duty cycle required in the application.

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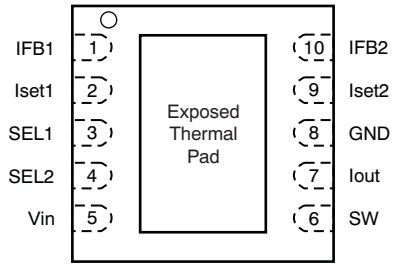
## DEVICE INFORMATION

**QFN-10 PACKAGE**
**3 mm ×3 mm**
**(TOP VIEW)**




## PIN DESCRIPTIONS

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| Vin | 5 | I | The input pin to the IC. It provides the current to the boost power stage, and also powers the IC circuit. When Vin is below the undervoltage lockout threshold, the IC turns off and disables outputs; thereby disconnecting the WLEDs from the input. |
| GND | 8 | O | The ground of the IC. Connect the input and output capacitors very close to this pin. |
| SW | 6 | I | This is the switching node of the IC. |
| Iout | 7 | O | The output of the constant current supply. It is directly connected to the boost converter output. |
| IFB1, IFB2 | 10 | I | The return path for the Iout regulation. Current regulator is connected to this pin, and it can be disabled to open the current path. |
| ISET1,<br>ISET2 | 2<br>9 | I | Output current programming pin. The resistor connected to the pin programs its corresponding output current. |
| SEL1,<br>SEL2 | 3<br>4 | I | Mode selection pins. See Table 1 for details. |
| Thermal Pal | | | The thermal pad should be soldered to the analog ground. If possible, use thermal via to connect to ground plane for ideal power dissipation. |

**Table 1. TPS61150/1 Mode Selection**

| SEL1 | SEL2 | IFB1 | IFB2 |
|---|---|---|---|
| H | L | Enable | Disable |
| L | H | Disable | Enable |
| H | H | Enable | Enable |
| L | L | IC Shutdown | |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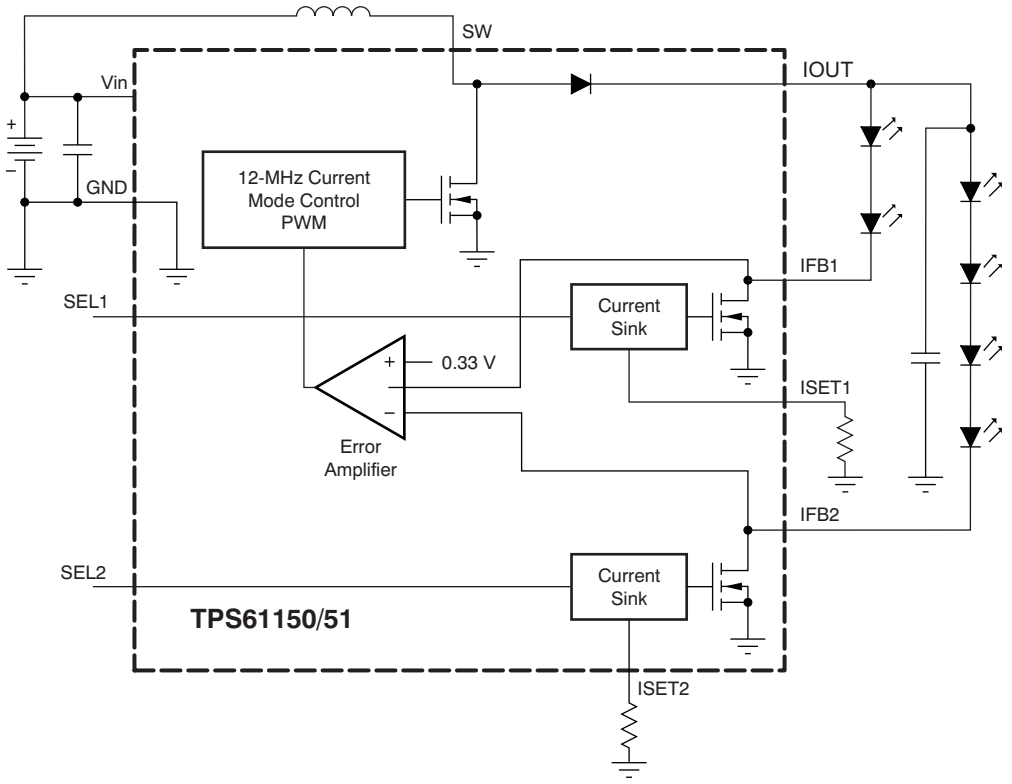
## FUNCTIONAL BLOCK DIAGRAM




## TYPICAL CHARACTERISTICS(1)

### Table of Graphs

| | | FIGURE |
|---|---|---|
| Overcurrent limit | $V_{IN}$ = 3 V, 3.6 V, and 4 V, Single and dual output | Figure 1, Figure 2 |
| WLED efficiency | $V_{IN}$ = 3.3 V, 3.6 V and 4 V, 3 WLED, WLED voltage= 11 V | Figure 3 |
| WLED efficiency | $V_{IN}$ = 3.3 V, 3.6 V and 4 V, 4 WLED, WLED voltage = 15 V | Figure 4 |
| WLED efficiency | $V_{IN}$ = 3.3 V, 3.6 V and 4 V, 5 WLED, WLED voltage = 19 V | Figure 5 |
| WLED efficiency | $V_{IN}$ = 3.3 V, 3.6 V and 4 V, 6 WLED, WLED voltage= 23 V | Figure 6 |
| Both on efficiency | $V_{IN}$ = 3.3 V, 3.6 V and 4 V, 4 WLED on each output | Figure 7 |
| K value over current | $V_{IN}$ = 3.6 V, $I_{LOAD}$ = 2 mA to 25 mA | Figure 8 |
| PWM dimming linearity | Frequency = 20 kHz and 30 kHz | Figure 9 |
| Single output PWM dimming waveform | | Figure 10 |
| Multiplexed PWM dimming waveform | | Figure 11 |
| Start-up waveform | | Figure 12 |

(1) Data for all characteristic graphs were taken using the typical application circuit on the front page of this data sheet with inductor = 10 µH (VLCF4018T-100MR74-2), R1 = R2 = 56kΩ, unless otherwise noted.

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## TYPICAL CHARACTERISTICS

OVERCURRENT LIMIT (SINGLE OUTPUT) VS DUTY CYCLE

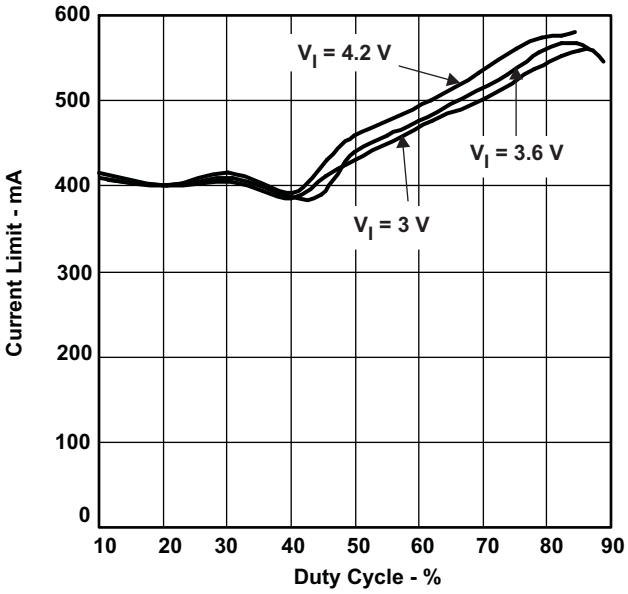


Figure 1.

OVERCURRENT LIMIT (DUAL OUTPUT) VS DUTY CYCLE

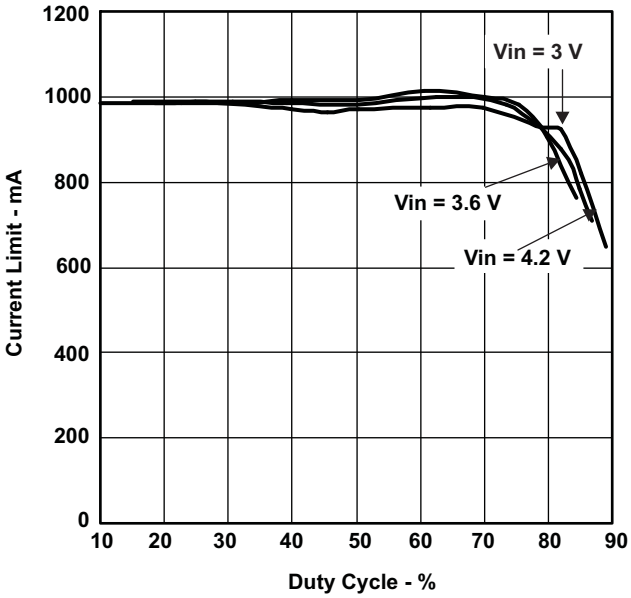


Figure 2.

EFFICIENCY VS LOAD CURRENT

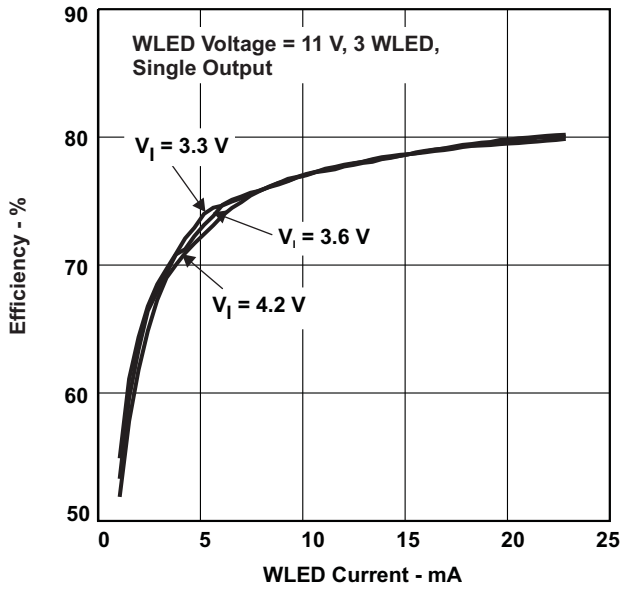


Figure 3.

EFFICIENCY VS LOAD CURRENT

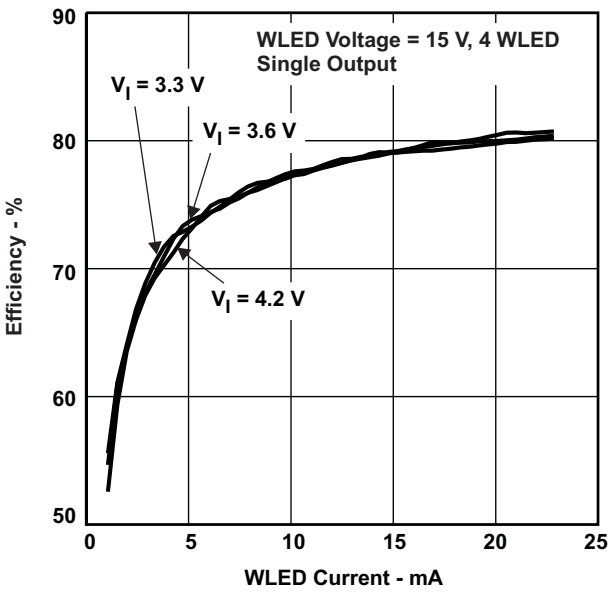


Figure 4.


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## TYPICAL CHARACTERISTICS (continued)

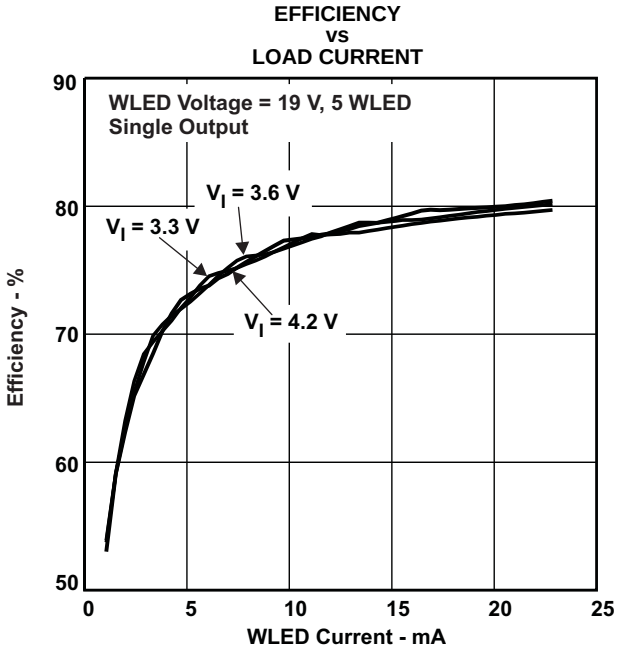


Figure 5.

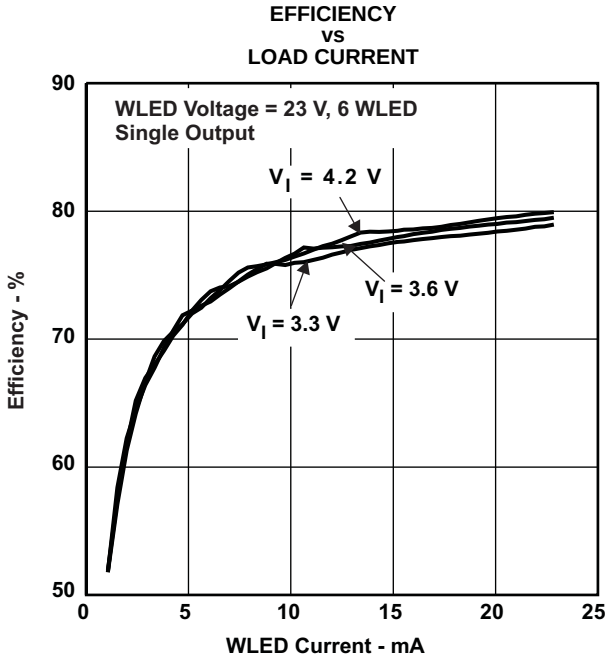


Figure 6.

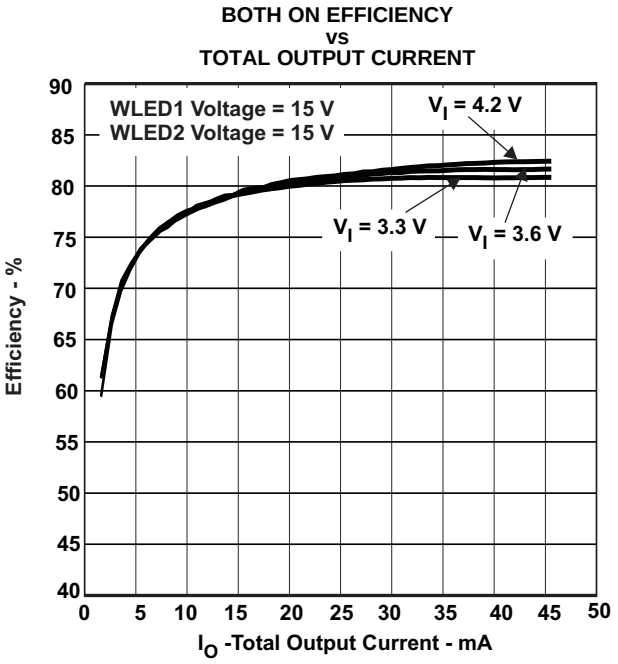


Figure 7.

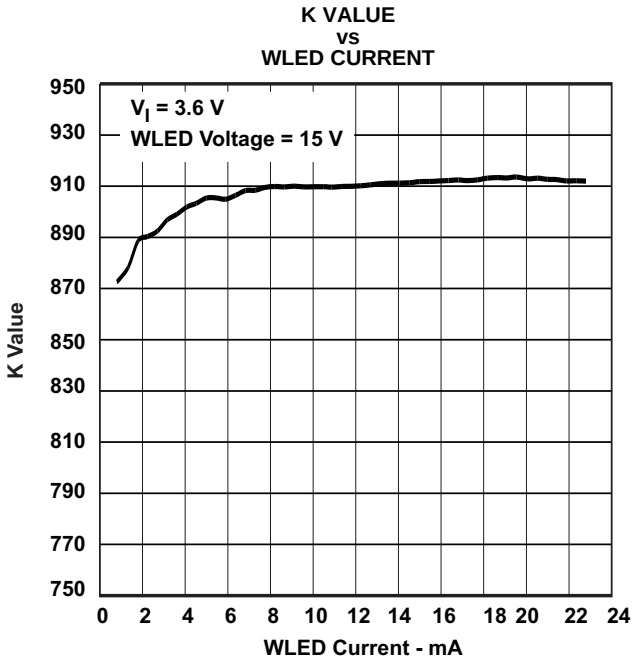


Figure 8.

## TYPICAL CHARACTERISTICS (continued)

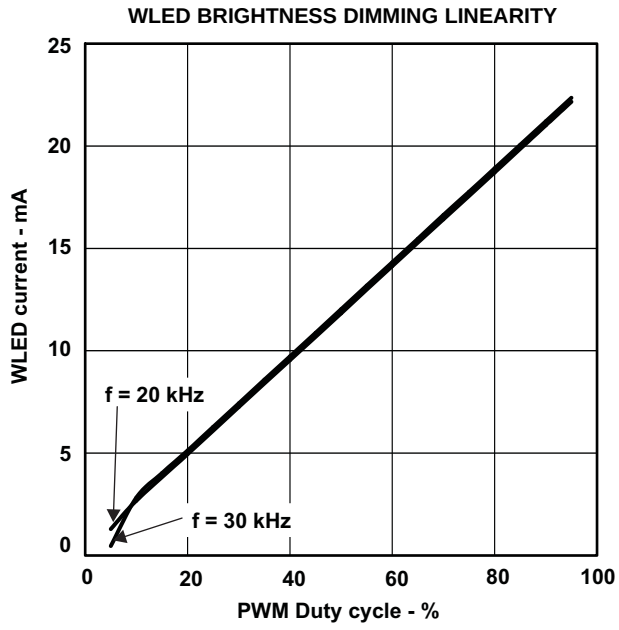


Figure 9.

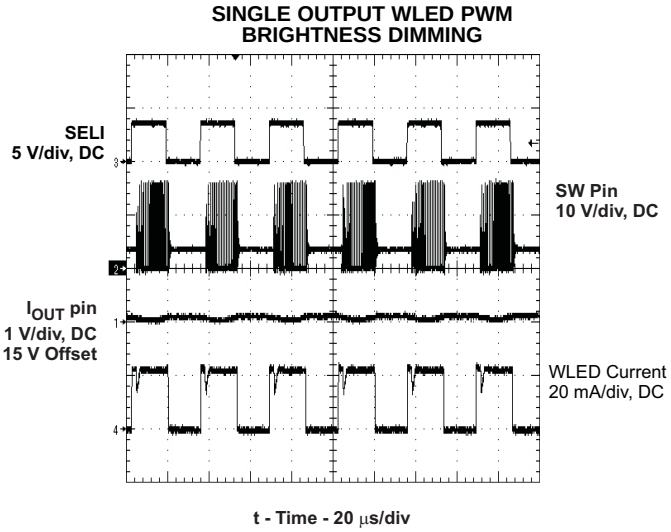


Figure 10.

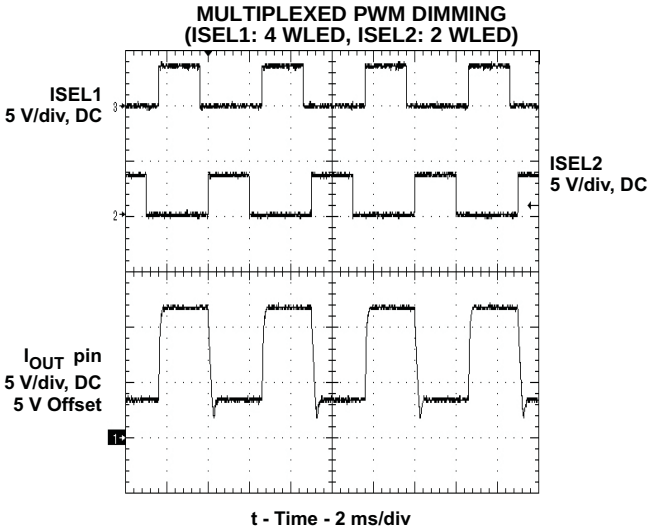


Figure 11.

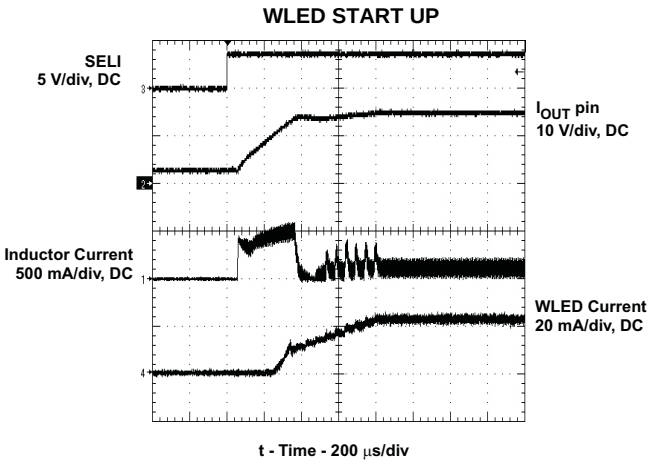


Figure 12.


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# DETAILED DESCRIPTION

## CURRENT REGULATION

The TPS61150/1 uses a single boost regulator to drive two WLED strings whose current can be programmed independently. The boost converter adopts PWM control which is ideal for high output current and low output ripple noises. The feedback loop regulates the IFB pins to a threshold voltage (330 mV typical), giving the current sink circuit just enough headroom to operate.

The regulation current is set by the resistor on the Iset pin based on Equation 1.

$$I_O = \frac{V_{ISET}}{R_{SET}} \times K_{ISET} \quad (1)$$

Where:

- $I_O$ = output current
- $V_{ISET}$ = Iset pin voltage (1.229 V typical)
- $R_{SET}$ = Iset pin resistor value
- $K_{ISET}$ = current multiplier (900 typical)

When both outputs are enabled, the boost converter provides enough power to provide the demanded current through IFB1 and IFB2 while keeping the voltage at IOUT [V(IOUT)] high enough to meet the forward voltage drops of the WLEDs. Specifically, at start up, the boost converter increases its output power, and therefore the output voltage, from IOUT until IFB1 reaches its regulated voltage. Once IFB1 is within regulation, the IC looks to the IFB2 voltage and may increase V(IOUT) further to get IFB2 in regulation. After both IFB pins reach regulation, the feedback path dynamically switches to whichever IFB pin drops more than the IFB low hysteresis voltage (60 mV typical) below its regulation voltage. This architecture ensures proper current regulation for both IFB1 pins; however, the voltage at one IFB pin will be higher than the minimum required regulation voltage. The overall efficiency when both strings are on depends on the voltage difference between the IFB1 and IFB2 pins. A large difference reduces the efficiency as a result of power losses across the current sink circuit of the IFB pin with the higher drop.

## START UP

During start up, both the boost converter and the current sink circuitry try to establish a steady state simultaneously. The current sink circuitry ramps up current in 16 steps, with each step taking 64 clock cycles. This period ensures that the current sink loop is slower than the boost converter response during start up. Therefore, the boost converter output comes up slowly as current sink circuitry ramps up the current. This configuration ensures a smooth start up and minimizes in-rush current.

## OVERVOLTAGE PROTECTION

To prevent the boost output runaway as the result of WLED disconnection, there is an overvoltage protection circuit that stops the boost converter from switching as soon as its output exceeds the OVP threshold. When the voltage falls below the OVP threshold, the converter resumes switching.

The two OVP options offer the choices to prevent a 25-V rated output capacitor or the internal 30-V FET from breaking down.

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## UNDERVOLTAGE LOCKOUT

An undervoltage lockout prevents device malfunction at input voltages below 1.65 V (typical). When the input voltage is below the undervoltage threshold, the device remains off and both the boost converter and current sink circuit are turned off, providing isolation between input and output.

## THERMAL SHUTDOWN

An internal thermal shutdown turns off the IC when the typical junction temperature of 160°C is exceeded. The thermal shutdown has a hysteresis of typically 15°C.

## ENABLE

Pulling either the SEL1 or SEL2 pin low turns off the corresponding output. If both SEL1 and SEL2 are low for more than 40 ms, the IC shuts down and consumes less than 1 μA current. The SEL pin can also be used for PWM brightness dimming. To improve PWM dimming linearity, soft start is disabled if the time between the falling and rising edges of two adjacent SELx pulses is less than 40 ms. See the *Application Information* section for details.

Each SEL input pin has an internal pulldown resistor to disable the device when the pin is floating.


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# APPLICATIONS INFORMATION

## MAXIMUM OUTPUT CURRENT

The over-current limit in a boost converter limits the maximum input current (and thus, the maximum input power) for a given input voltage. Maximum output power is less than the maximum input power because of power conversion losses. Therefore, the current limit, input voltage, output voltage, and efficiency can all change maximum current output. Because current limit clamps peak inductor current, ripple must be subtracted to derive the maximum dc current. The ripple current is a function of switching frequency, inductor value, and duty cycle. The following equations take all of the above factors into account for maximum output current calculation.

$$I_p = \frac{1}{\left[L \times \left(\frac{1}{Viout + Vf - Vin} + \frac{1}{Vin}\right) \times Fs\right]} \quad (2)$$

Where:

- $I_p$ = inductor peak to peak ripple
- L = inductor value
- Vf = power diode forward voltage
- Fs = switching frequency
- Viout = boost output voltage. It is equal to 330 mV + voltage drop across WLED.

$$Iout_max = \frac{Vin \times \left(Ilim - \frac{I_p}{2}\right) \times \eta}{Viout} \quad (3)$$

Where:

- Iout_max = maximum output current of the boost converter
- Ilim = overcurrent limit
- $\eta$ = efficiency

To keep a tight range on the overcurrent limit, the TPS61150/1 uses the Vin and Iout pin voltage to compensate for the overcurrent limit variation caused by the slope compensation. However, the current threshold still has a residual dependency on the Vin and Iout voltage. Use Figure 1 and Figure 2 to identify the typical overcurrent limit in your specific application, and use a ±25% tolerance to account for temperature dependency and process variations.

The maximum output current can also be limited by the current capability of the current sink circuitry. It is designed to provide a maximum 35-mA current regardless of the current capability of the boost converter.

## WLED BRIGHTNESS DIMMING

There are three ways to change the output current *on the fly* for WLED dimming. The first method parallels an additional resistor with the ISET pin resistor as shown in Figure 13. The switch (Q1) can change the ISET pin resistance, and therefore modify the output current. This method is very simple, but can only provide limited dimming steps.

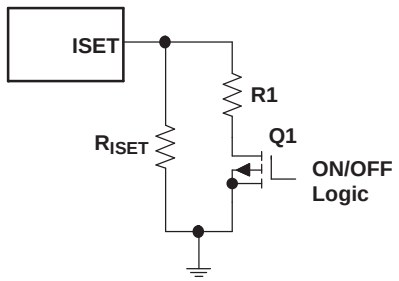


**Figure 13. Switching In/Out an Additional Resistor to Change Output Current**

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Alternatively, a PWM dimming signal at the SEL pin can modulate the output current by the duty cycle of the signal. The logic high of the signal turns on the current sink circuit, while the logic low turns it off. This operation creates an averaged dc output current proportional to the duty cycle of the PWM signal. The frequency of the PWM signal must be high enough to avoid flashing of the WLEDs. The soft start of the current sink circuit is disabled during the PWM dimming to improve linearity.

The major concern of the PWM dimming is the creation of audible noises that can come from the inductor and/or output capacitor of the boost converter. The audible noises on the output capacitor are created by the presence of voltage ripple in range of audible frequencies. The TPS61150/1 alleviates the problem by disconnecting the WLEDs from the output capacitor when the SEL pin is low. Therefore, the output capacitor is not discharged by the WLEDs, and thus reduces the voltage ripple during PWM dimming.

The audible noises can be eliminated by using a PWM dimming frequency above or below the audible frequency range. The maximum PWM dimming frequency of the TPS61150/1 is determined by the current settling time ($T_{isink}$), which is the time required for the sink circuit to reach a steady state after the SEL pin transitions from low to high. The maximum dimming frequency can be calculated by Equation 4:

$$F_{PWM_MAX} = \frac{D_{min}}{T_{isink}} \tag{4}$$

Where:

- $D_{min}$ = min duty cycle of the PWM dimming required in the application

For 20% $D_{min}$, a PWM dimming frequency up to 33 kHz is possible, putting the noise frequency above the audible range.

Because the TPS61150/1 dynamically regulates one IFB pin voltage, its output voltage can have a large ripple during PWM dimming as shown in Figure 11. This ripple may cause ceramic output capacitors to ring audibly. To reduce the output ripple, the configurations shown in Figure 15 and Figure 16 are recommended for PWM dimming. In Figure 15, both current strings have the same number of LEDs and the same PWM signal. In Figure 16, one string (in this case, string 2) is not PWM dimmed and has a greater total forward voltage drop than string 1, either because of having more LEDs than string 1 or because of adding a resistor in series with string 2. Therefore, IFB2 controls the regulation regardless of the PWM signal on IFB1 and the output ripple is significantly reduced when string 1 is dimmed. The circuit in Figure 16 could have been reconfigured with string 1 having the larger total forward drop.

The third method uses an external dc voltage and resistor as shown in Figure 14 to change the ISET pin current, and thus control the output current. The dc voltage can be the output of a filtered PWM signal. The equation to calculate the output current is given by Equation 5 and Equation 6.

$$I_{WLED} = K_{ISET} \times \left( \frac{1.229}{R_{ISET}} + \frac{1.229 - V_{DC}}{R_1} \right) \text{ for DC voltage input} \tag{5}$$

$$I_{WLED} = K_{ISET} \times \left( \frac{1.229}{R_{ISET}} + \frac{1.229 - V_{DC}}{R_1 + 10K} \right) \text{ for PWM signal input} \tag{6}$$

Where:

- $K_{ISET}$ = current multiplier between the ISET pin current and the IFB pin current.
- $V_{DC}$= voltage of the dc voltage source or the dc voltage of the PWM signal.

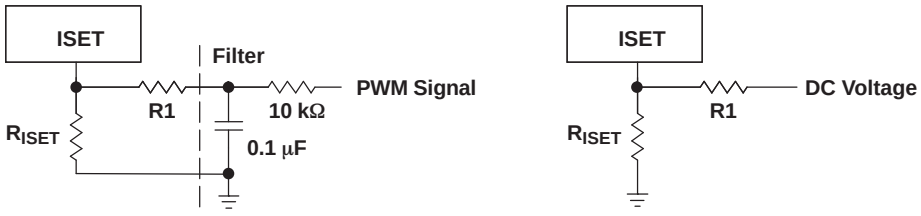


**Figure 14. Analog Dimming Uses an External Voltage Source to Control the Output Current**


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## INDUCTOR SELECTION

Because the selection of the inductor affects the power supply steady-state operation, transient behavior, and loop stability, the inductor is the most important component in power regulator design. Three specifications are the most important to the performance of the inductor: the inductor value, dc resistance, and saturation current. Considering the inductor value alone is not enough.

The inductor inductance value determines the inductor ripple current. It is generally recommended to set peak-to-peak ripple current given by Equation 2 to betweeen 30% to 40% of dc current. It is a good compromise of power loss and inductor size. For this reason, 10-µH inductors are recommended for the TPS61150/1. Inductor dc current can be calculated as Equation 7.

$$I_{L_DC} = \frac{V_{iout} \times I_{out}}{V_{in} \times \eta} \quad (7)$$

Use the maximum load current and minimum $V_{in}$ for calculation.

The internal loop compensation for PWM control is optimized for the external component shown in the Typical Application Circuit with consideration of component tolerance. Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0-A value. depending on how the inductor vendor defines saturation. Using an inductor with a smaller inductance value forces discontinuous PWM in which the inductor current ramps down to zero before the end of each switching cycle. It reduces the boost converter maximum output current, and causes large input voltage ripple. An inductor with larger inductance will reduce the gain and phase margin of the feedback loop, possibly resulting in instability.

Regulator efficiency depends on the resistance of its high current path and switching losses associated with the PWM switch and power diode. Although the TPS61150/1 has optimized the internal switches, the overall efficiency still relies on inductor dc resistance (DCR); lower DCR improves efficiency. However, there is a trade-off between DCR and inductor size, and shielded inductors typically have higher DCR than unshielded ones. A DCR in range of 150 mΩ to 350 mΩ is suitable for applications that require *both on* mode. A DCR is the range of 250 mΩ to 450 mΩ is a good choice for single output applications. Table 2 and Table 3 list some recommended inductor models.

**Table 2. Recommended Inductors for Single Output**

| | L (µH) | DCR Typ (mΩ) | Isat (A) | SIZE (L×W×H mm) |
|---|---|---|---|---|
| **TDK** | | | | |
| VLF3012AT-100MR49 | 10 | 360 | 0.49 | 2.8×3.0×1.2 |
| VLCF4018T-100MR74-2 | 10 | 163 | 0.74 | 4.0×4.0×1.8 |
| **Sumida** | | | | |
| CDRH2D11/HP | 10 | 447 | 0.52 | 3.2×3.2×1.2 |
| CDRH3D16/HP | 10 | 230 | 0.84 | 4.0×4.0×1.8 |

**Table 3. Recommended Inductors for Dual Output**

| | L (µH) | DCR Typ (mΩ) | Isat (A) | SIZE (L×W×H mm) |
|---|---|---|---|---|
| **TDK** | | | | |
| VLCF4018T-100MR74-2 | 10 | 163 | 0.74 | 4×4.0×1.8 |
| VLF4012AT-100MR79 | 10 | 300 | 0.85 | 3.5×3.7×1.2 |
| **Sumida** | | | | |
| CDRH3D16/HP | 10 | 230 | 0.84 | 4×4.0×1.8 |
| CDRH4D11/HP | 10 | 340 | 0.85 | 4.8×4.8×1.2 |

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## INPUT AND OUTPUT CAPACITOR SELECTION

The output capacitor is primarily selected for the output ripple of the converter. This ripple voltage is the sum of the ripple caused by the capacitor capacitance and its equivalent series resistance (ESR). Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by Equation 8.

$$C_{out} = \frac{\left(V_{iout} - V_{in}\right) I_{out}}{V_{iout} \times Fs \times V_{ripple}} \quad (8)$$

Where:

- $V_{ripple}$ = Peak to peak output ripple

For $V_{in}$ = 3.6 V, $V_{iout}$ = 20 V, and $F_s$ = 1.2 MHz, 0.1% ripple (20 mV) would require a 1-µF capacitor. For this value, ceramic capacitors are the best choice for size, cost, and availability.

The additional output ripple component caused by ESR is calculated using the equation:

$$V_{ripple_ESR} = I_{out} \times R_{ESR}$$

As a result of its low ESR, $V_{ripple_ESR}$ can be neglected for ceramic capacitors, but must be considered if tantalum or electrolytic capacitors are used.

During a load transient, the capacitor at the output of the boost converter must supply or absorb additional current before the inductor current ramps up the steady-state value. Larger capacitors always help to reduce the voltage over-and undershoot during a load transient. A larger capacitor also helps loop stability.

Care must be taken when evaluating ceramic capacitor derating because of the applied dc voltage, aging, and frequency response. For example, larger form factor capacitors (in size 1206) have self-resonant frequencies in the range of the TPS61150/1 switching frequency. Therefore, the effective capacitance is significantly lower for these capacitors. As a result, it may be necessary to use small capacitors in parallel instead of one large capacitor.

Table 4 lists some recommended input and output ceramic capacitors. Two popular vendors for high-value ceramic capacitors are:

TDK (http://www.component.tdk.com/components.php)

Murata (http://www.murata.com/cap/index.html)

**Table 4. Recommended Input and Output Capacitors**

| | Capacitance (µF) | Voltage (V) | Case |
|---|---|---|---|
| **TDK** | | | |
| C3216X5R1E475K | 4.7 | 25 | 1206 |
| C2012X5R1E105K | 1 | 25 | 805 |
| C1005X5R0J105K | 1 | 6.3 | 402 |
| **Murata** | | | |
| GRM319R61E475KA12D | 4.7 | 25 | 1206 |
| GRM216R61E105KA12D | 1 | 25 | 805 |
| GRM155R60J105KE19D | 1 | 6.3 | 402 |

## LAYOUT CONSIDERATIONS

As for all switching power supplies, especially those providing high current and using high switching frequencies, printed circuit board (PCB) layout is an important design step. If layout is not carefully done, the regulator could show instability as well as electromagnetic interference (EMI) problems. Therefore, use wide and short traces for high current paths. The input capacitor must not only be close to the Vin pin, but also to the GND pin in order to reduce the input ripple seen by the IC. The Vin and SW pins are conveniently located on the edges of the IC; therefore, the inductor can be placed close to the device. The output capacitor must be placed near the load to minimize ripple and maximize transient performance.


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It is also beneficial to have the ground of the output capacitor close to the GND pin because there will be a large ground return current flowing between these two connections. When laying out the signal ground, use short traces separated from power ground traces, and connect them together at a single point on the PCB.

## ADDITIONAL APPLICATION CIRCUITS

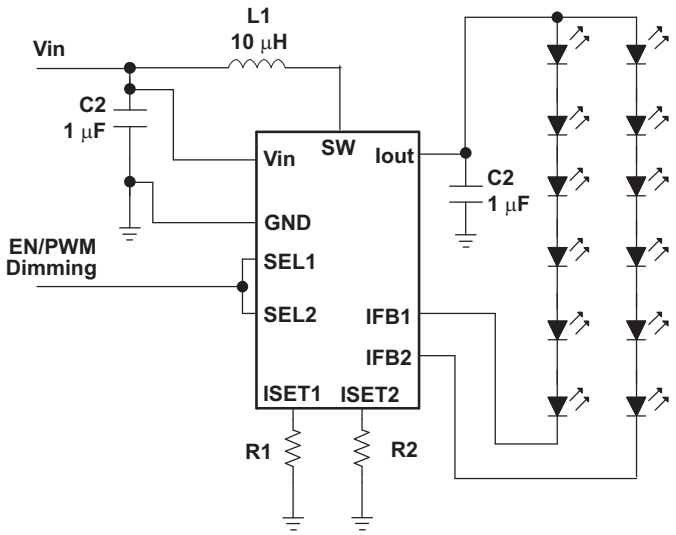


**Figure 15. Driving Up to 12 WLEDs With One LCD Backlight**

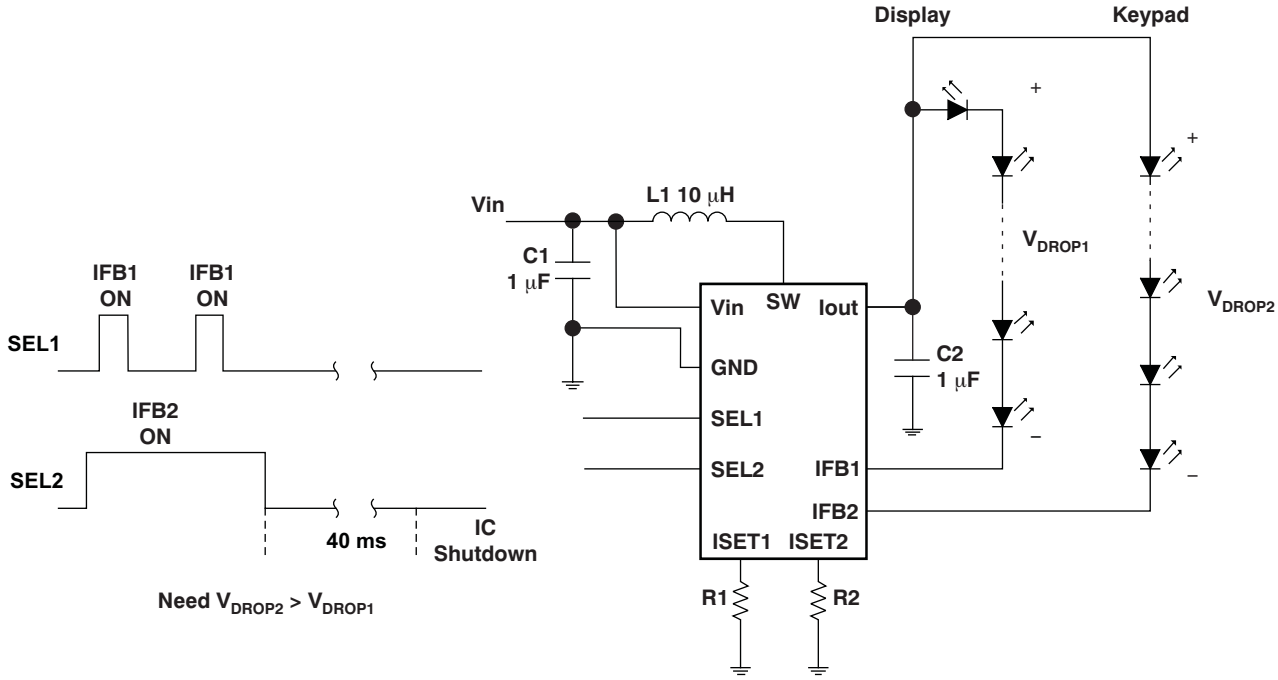


**Figure 16. Driving a Keypad and LCD Backlight, Applying PWM Signal to the SEL1 Pin**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| TPS61150DRCR | ACTIVE | SON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS61150DRCRG4 | ACTIVE | SON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS61150DRCRT | PREVIEW | SON | DRC | 10 | | TBD | Call TI | Call TI |
| TPS61150DRCT | ACTIVE | SON | DRC | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS61150DRCTG4 | ACTIVE | SON | DRC | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS61151DRCR | ACTIVE | SON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS61151DRCRG4 | ACTIVE | SON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS61151DRCT | ACTIVE | SON | DRC | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS61151DRCTG4 | ACTIVE | SON | DRC | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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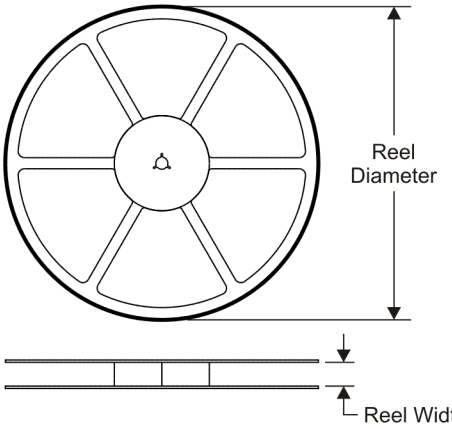
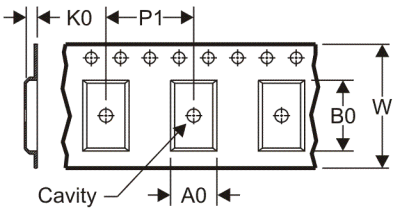
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

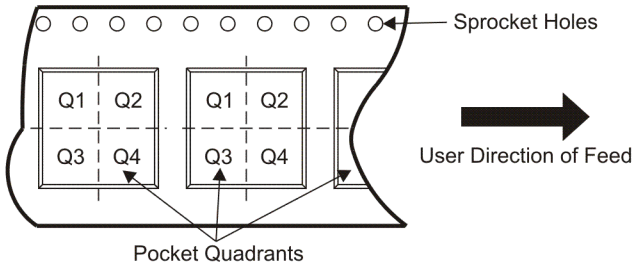



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

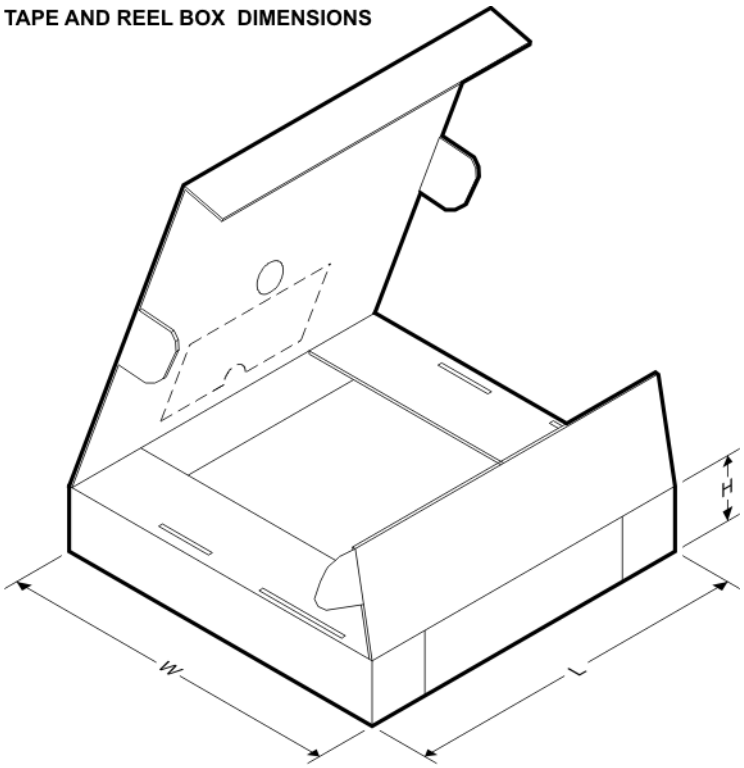
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS61150DRCR | SON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS61151DRCR | SON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS61151DRCT | SON | DRC | 10 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

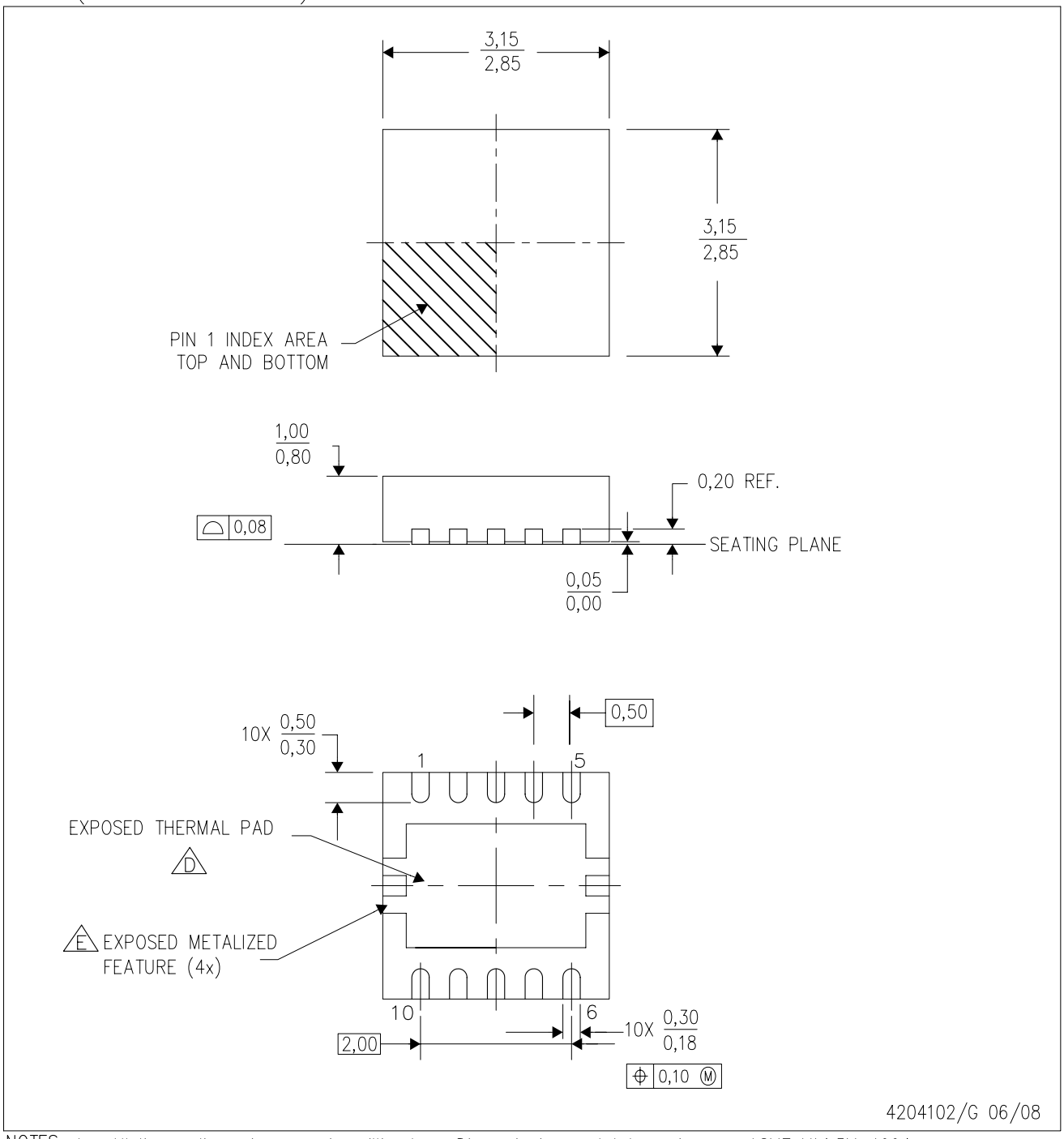
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS61150DRCR | SON | DRC | 10 | 3000 | 346.0 | 346.0 | 29.0 |
| TPS61151DRCR | SON | DRC | 10 | 3000 | 346.0 | 346.0 | 29.0 |
| TPS61151DRCT | SON | DRC | 10 | 250 | 190.5 | 212.7 | 31.8 |

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Metalized features are supplier options and may not be on the package.

# THERMAL PAD MECHANICAL DATA

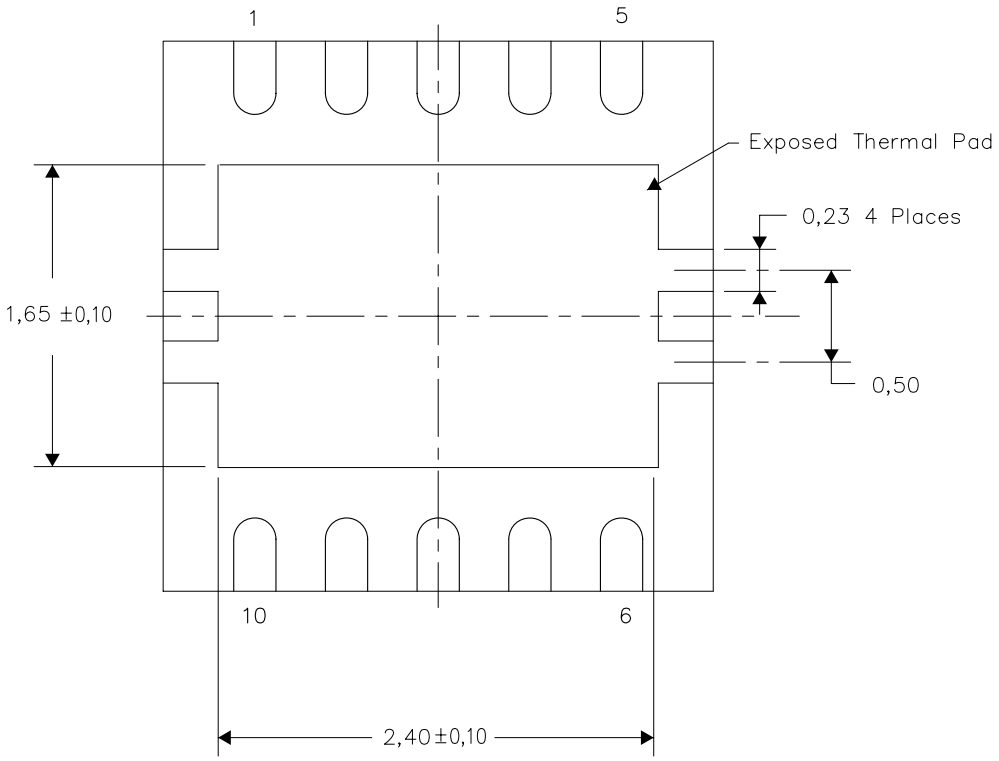
DRC (S–PVSON–N10)

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

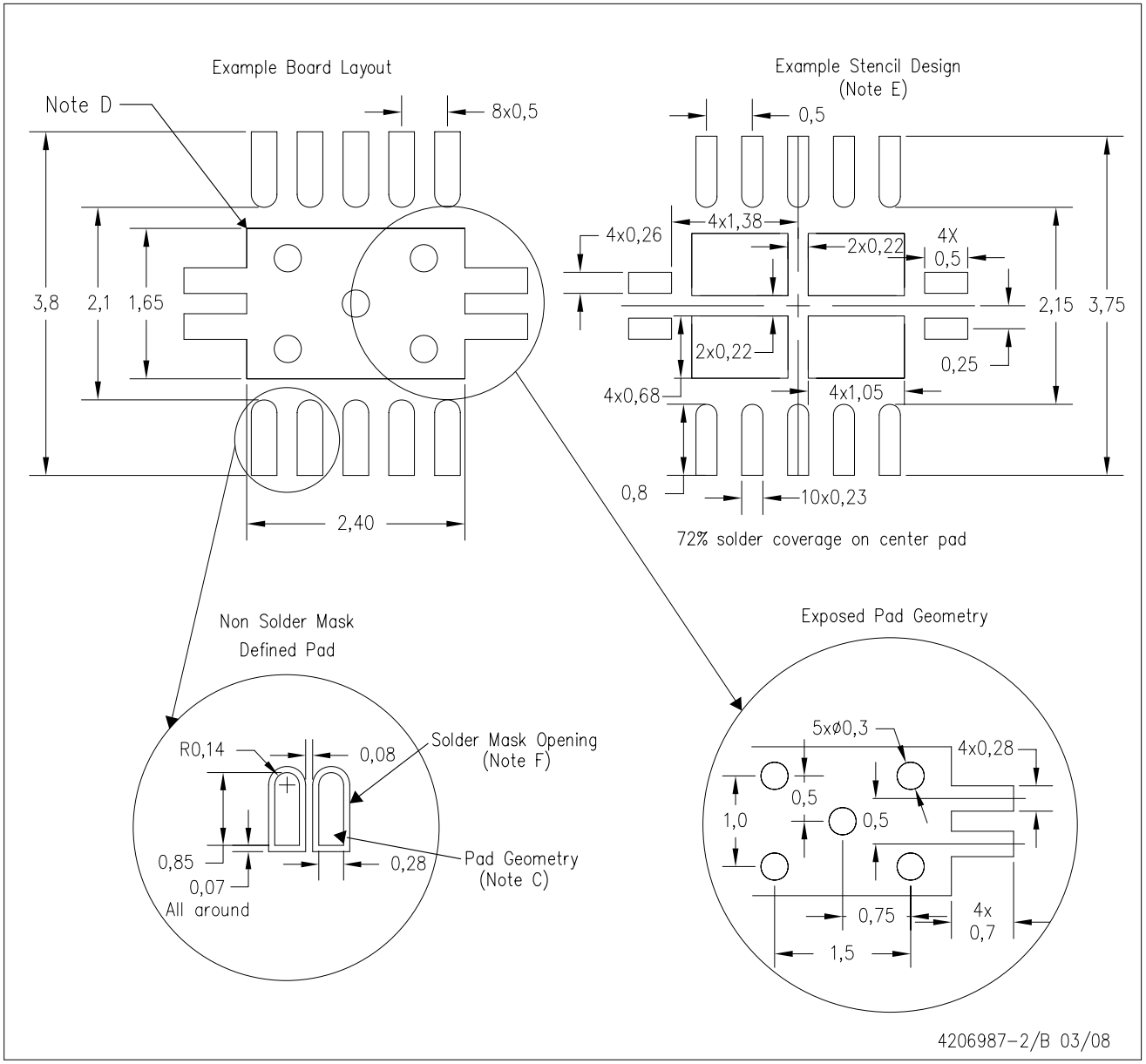



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

# DRC (S–PVSON–N10)




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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